**ECE 3220 VHDL**

**Catalog Description**

**ECE 3220 VHDL (4)**

Introduces logic system design using a hardware description language (VHDL). Covers the VHDL language in depth and explains how to use it to describe complex combinational and sequential logic circuits. Include a weekly lab where students will get hands-on experience implementing digital systems on Field Programmable Gate Arrays.

**Prerequisite:** ECE 2070 and ECE 3200.

**Prerequisite by topic:**

Programming Skill

Electronics

Digital Circuits

**Units and Contact Time:** 4 semester units: 3 units lecture (150 minutes), 1 unit lab (150 minutes).

**Type:** Required for CE. Selected elective for EE.

**Required Textbook:**

Digital Fundamentals with VHDL. Thomas L. Floyd. ISBN-10: 0130995274 | ISBN-13: 9780130995278. Prentice Hall. This book is available in the CSUB Bookstore and at retail and Internet bookstores.

**Recommended Textbook and Other Supplemental Materials:**

RTL Harware Design Using VHDL: Coding for Efficiency, Portability, and Scalability. Pong P. Chu. ISBN-13: 978-0-471-72092-8, ISBN-10: 0-471-72092-5

**Coordinator(s)**

Wei Li

**Student Learning Outcomes**

This course covers the following ACM/IEEE Body of Knowledge student learning outcomes:

CS-PL. Programming Languages

CE-DIG: Digital Logic

CE-CAO: Computer Architecture and Organization

ABET Outcome Coverage

The course maps to the following performance indicators for Computer Science (CAC/ABET) and Computer Engineering (EAC/ABET) and Electrical Engineering (EAC/ABET):

1. Analyze a problem, and identify and define the computing requirements and specifications appropriate to its solution (EAC 3b).
2. Identify, formulate, and solve engineering problems (EAC 3e).
3. Write a professional project report that presents the outcomes of the project and present these findings to the class (EAC 3g).

4. Use modern engineering tools such as ISO, FPGA Board, and Virtual Digital Instruments, to complete the assigned project (EAC 3k)

**Lecture Topics and Rough Schedule**

Week 01 Introduction/ISE

Week 02 Introduction to Digital Design

Week 03 Overview of VHDL

Week 04 Basic Language Constructs

Week 05 Concurrent Signal Assignment Stmts

Week 06 Sequential Statements in VHDL and Synthesis of VHDL Code

Week 07 Combinational Circuit Design: Project Design 1

Week 08 Sequential Circuit Design: Principle Sequential Circuit

Week 09 Sequential Circuit Design: Project Design 2

Week 10 Sequential Circuit Design: Project Design 3

Week 11 Finite State Machines Simple FSM

Week 12 Complex Sequential Circuit Design: Project Design 4

Week 13 Hierarchical Design in VHDL: Project 5

Week 14 Parameterized Design

Week 15 Clock Synchronization: Project Design 6

**Grading Policy**

 A 93%

A- 90%

 B+ 87%

 Lab/Hw Assignments ....35% B 83%

 Midterm 1 ......................20% B- 80%

 Midterm 2 ......................20% C+ 77%

 Final Project....................25% C 73%

 C- 70%

 D+ 67%

 D 63%

 D- 60%

 F below 60%

**Prepared By**

Wei Li on June 11, 2014

**Approval**

Approved by CEE/CS Department on July 30, 2014

**Effective Fall 2016**